REMARKS

This Amendment is in response to the Office Action mailed 6/23/2005. In the Office Action, claims 1-30 were rejected under 35 U.S.C. § 103. Claims 1, 11 and 21 have been amended with the amendments being fully supported by the specifications and introducing no substantive new matter. The Amendment is concurrently filed with a Request for Continued Examination (RCE). Reconsideration in light of the foregoing amendments and following remarks made herein is respectfully requested.

Claims 1-30 remain in this application.

Rejection Under 35 U.S.C. § 103

Claims 1, 11, and 21 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Yeager et al. ("Yeager") (5,758,112) in view of Christie et al ("Christie") (2004/0186981).

As the Examiner is aware, to establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify a reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all of the claim limitations. *See MPEP §2143; see also In Re Fine, 873 F. 2d 1071, 5 U.S.P.Q.2d 1596 (Fed. Cir. 1988).* Herein, at a minimum, the combined teachings of the cited references do not describe or suggest all the claim limitations for each of claims 1, 11 and 21.

In general, with respect to amended claim 1, Yeager does not disclose, either expressly or inherently: (i) determining via a binary translation process a last use of a first canonical register in a block of code after a renaming, the first canonical register being mapped to a first original register; and (ii) applying one of a first rollback and a first recovery via the binary translation process to the first original register based on whether the determined last use of the first canonical register occurs before a last definite write to the first original register in the block of code (emphasis added).

In one embodiment of the claimed invention, the decision on whether to apply a rollback or recovery is first based on a determination of a last use of a first canonical register (i.e. the last time a canonical register was read from) as illustrated in the example provided in prg [0041] of the detail description and the accompanying description beginning on prg [0042]. The decision on whether to apply a rollback or recovery is also based on whether the determined last use of the first canonical register occurs before a last definite write to the first original register in the block of code.

In addition, Yeager is directed to a superscalar processor architecture in which redundant mapping tables are used to rename registers and perform branch prediction. It is well known in the art that superscalar processor architecture operates on a different basis than a binary translation processor as is used in the claimed embodiment of the invention. In a superscalar architecture, state recovery problems are addressed via a dynamic approach by mapping between renamed registers and renaming registers using additional hardware, such as RAM. In a binary translation process,

however, every instruction is generally translated only once (or a limited number of times) in which the dynamic approach and additional hardware of the superscalar architecture proves wasteful.

Yeager merely describes a superscalar processor wherein redundant RAM cells can dynamically restore primary RAM cells in a single clock cycle should a branch instruction be misinterpreted. Yeager is thus silent as to determining based on a binary translation process a last use of a canonical register and then to condition the application of a rollback or recovery operation on whether the determined last use of the canonical register occurs before a last definite write to the original register. In this regard it was stated on page 6 of the Office Action that columns 7, lines 53-55 disclose the foregoing feature of the present invention. Applicant respectfully disagrees. At the cited reference, Yeager merely discloses a mapping table which reflects the latest mapping of logical destination register number wherein the old physical destination associated with logical number is outputted from mapping table and appended to an active list. No mention of a determining based on a binary translation process a last use of a first canonical register and then conditioning the application of a rollback or recovery operation on whether the determined last use of the first canonical register occurs before a last definite write to the original register in the block of code, is found in the cited reference or anywhere in Yeager. Thus, Yeager does not disclose the foregoing feature of claim 1. Christie is likewise silent on the foregoing feature of claim 1.

Therefore, Yeager and Christie, taken alone or in any combination, do not disclose or render obvious: determining based on a binary translation process a last use of a first canonical register in a block of code after a renaming, the first canonical register being mapped to a first original register; and applying one of a first rollback and a first recovery based on the binary translation process to the first original register based on whether the determined last use of the first canonical register occurs before a last definite write to the first original register in the block of code. As a result, a *prima facie* case of obviousness has not been established.

Applicant respectfully requests that the Examiner withdraw the outstanding §103(a) rejection of claim 1.

Amended independent claims 11 and 21 are directed to a computer program product and system, respectively, and which each share the same novel features of claim 1. Therefore for at least the above-stated reasons with regard to the amended claim 1, Applicant submits that each of claims 11 and 21 are patentably distinguished over the prior art and are therefore not rendered obvious under §103(a).

Applicant respectfully requests that the Examiner withdraw the outstanding §103(a) rejection of claims 11 and 21.

Claims 2-10 ultimately depend from amended independent claim 1 and thus include all the limitations of amended claim 1, as well as reciting the above-described further limitations of particular utility. Therefore, for at least the above-stated reasons with regard to amended claim 1, the Applicant submits that claims 2-10 are patentably distinguished over the prior art. The applicant respectfully requests the Examiner to withdraw the outstanding §103(a) rejection of claims 2-10.

Claims 12-20 ultimately depend from amended independent claim 11 and thus include all the limitations of amended claim 11, as well as reciting the above-described further limitations of particular utility. Therefore, for at least the above-stated reasons with regard to amended claim 11, Applicant submits that claims 12-20 are patentably distinguished over the prior art. Applicant respectfully requests the Examiner to withdraw the outstanding §103(a) rejection of claims 12-20.

Claims 22-30 ultimately depend from amended independent claim 21 and thus include all the limitations of amended claim 21, as well as reciting the above-described further limitations of particular utility. Therefore, for at least the above-stated reasons with regard to amended claim 21, Applicant submits that claims 22-30 are patentably distinguished over the prior art. Applicant respectfully requests the Examiner to withdraw the outstanding §103(a) rejection of claims 22-30.

Conclusion

It is believed that this Amendment places the above-identified patent application into condition for allowance. Applicant respectfully requests that a timely Notice of Allowance be issued in this case.

Respectfully submitted,

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